



ChaCha20-Poly I 305 / Ascon

Symmetric Encryption

Product codes ChaCha20-Poly I 305: XIP2 I I 3B, XIP2 I I 3H Ascon: XIP220 I B

Xiphera's ChaCha20-Poly1305 and Ascon symmetric encryption IP cores provide robust security for a wide range of applications. ChaCha20-Poly1305 combines the high-speed ChaCha20 stream cipher with the Poly1305 authenticator, delivering both encryption and authentication. Ascon, as a lightweight encryption algorithm, is ideal for constrained environments such as IoT devices. Both of these Xiphera in-house designed IP cores are optimised for efficiency and optimal performance in both FPGA and ASIC implementations.

KEY FEATURES

- Optimised resource requirements
- High throughput up to 50 Gbps on ChaCha20-Poly I 305
- Compliant with modern cryptographic standards
- Quantum-secure
- Pure RTL without hidden CPU or software components
- Easy system integration
- Vendor agnostic FPGA/ASIC implementation

APPLICATIONS

Enhance your security with advanced encryption engines:

- Data centres and cloud environments
- IPsec/TLS/DTLS/SSH protocols
- Data communications
- IoT devices
- Wearables
- Low-power devices and constrained environments

ChaCha20-Poly I 305 / Ascon Symmetric Encryption

Our ChaCha20-Poly I 305 and Ascon IP cores provide versatile encryption solutions, ensuring optimal performance, flexibility, and robust security.

ChaCha20-Poly I 305

BALANCED

XIP2 | | 3B

- Several Gbps
- Only ~7.3 kLUTs

HIGH-SPEED

XIP2 | 13H

- 10s of Gbps
- ~24 kLUTs

Ascon

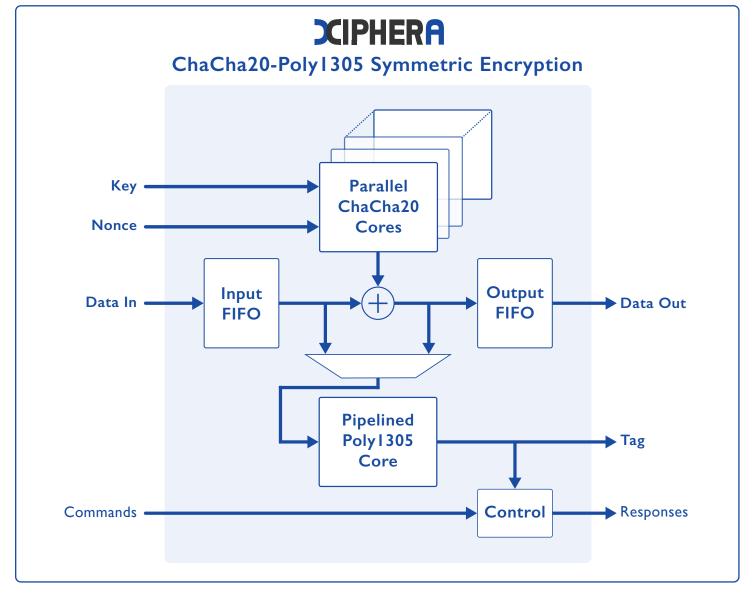
The lightweight Ascon algorithm is ideal for constrained environments, such as IoT devices.

BALANCED

XIP2201B

- 100s of Mbps
- Only ~2.3 kLUTs

We also offer AES symmetric encryption solutions. For more details, please see our dedicated product flyer.



Deliverables

⊘ Comprehensive simulation test bench, scripts & guide	○ Detailed datasheet and integration guide

About Xiphera

Xiphera, Ltd, is a Finnish company designing hardware-based security solutions using standardised cryptographic algorithms. Our product portfolio consists of secure and efficient cryptographic Intellectual Property (IP) cores, designed directly for ASICs and FPGAs. Our strong cryptographic expertise, extensive experience in system design, and deep knowledge in the field of reprogrammable logic enable us to offer our customers peace of mind in a dangerous world.

