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XIP8103H: PRNG

High-Speed AES-based Pseudorandom Number Generator

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP8103H with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP8103H.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera® Cyclone® 10 GX[†]	15209 ALM	297.53 MHz	37.65 Gbps
Altera® Agilex® 7 F[†]	18578 ALM	513.08 MHz	64.93 Gbps
AMD® Versal® Prime[‡]	17561 LUT	374.39 MHz	47.38 Gbps
AMD® Zynq® MPSoC[‡]	17733 LUT, 1 RAMB18	309.12 MHz	39.12 Gbps
Lattice® CertusPro-NX® [§]	32444 LUT4, 1 EBR	156.03 MHz	19.75 Gbps
Lattice® Avant® [§]	36192 LUT4, 1 EBR	158.00 MHz	19.99 Gbps
Microchip® PolarFire® [¶]	93046 4LUT, 12 uSRAM	226.30 MHz	28.64 Gbps

Table 1: Resource usage and performance of XIP8103H on various FPGA families.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.
[§]Radiant 2025.1.0, default compilation settings, industrial speedgrade.
[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP8103H on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP8103H with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
253133	65612	667 MHz

Table 2: Logic requirements and performance of XIP8103H on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP8103H.

Type	Address depth	Data Width (bits)	Total (bits)
SPRAM	16	128	2048
			2048

Table 3: Memory requirements of XIP8103H.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins.
[3] Target frequency. Does not account for routing delays.