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XIP8103B: PRNG

Balanced AES-based Pseudorandom Number Generator

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP8103B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP8103B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera® Agilex® 5†	3806 ALM, 4 M20K	264.90 MHz	1.54 Gbps
Altera® Cyclone® 10 GX†	3677 ALM, 4 M20K	288.02 MHz	1.68 Gbps
AMD® Versal® Prime‡	4233 LUT	403.88 MHz	2.35 Gbps
AMD® Zynq® MPSoC‡	4045 LUT, 1 RAMB18	347.10 MHz	2.02 Gbps
Lattice® CertusPro-NX® §	5888 LUT4, 5 EBR	120.74 MHz	702.51 Mbps
Lattice® Avant® §	6578 LUT4	212.50 MHz	1.24 Gbps
Microchip® PolarFire® ¶	14143 4LUT, 11 uSRAM	189.72 MHz	1.10 Gbps

Table 1: Resource usage and performance of XIP8103B on various FPGA families.

†Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
‡Vivado 2024.2, default compilation settings, industrial speedgrade.
§Radiant 2025.1.0, default compilation settings, industrial speedgrade.
¶Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP8103B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP8103B with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
29310	7597	667 MHz

Table 2: Logic requirements and performance of XIP8103B on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP8103B.

Type	Address depth	Data Width (bits)	Total (bits)
SPRAM	16	128	2048
			2048

Table 3: Memory requirements of XIP8103B.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.