XIPHERA

PEACE OF MIND IN A DANGEROUS WORLD

XIP8001B: TRNG

True Random Number Generator IP Core

Resource Sheet

2026-05-06

sales@xiphera.com

Introduction

This document details FPGA and ASIC resource requirements and performance of XIP8001B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP8001B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$
Altera® Cyclone® 10 GX[†]	1157 ALM, 2 M20K	352.61 MHz
Altera® Agilex® 5[†]	1218 ALM, 2 M20K	292.31 MHz
AMD® Versal® Prime[‡]	1641 LUT, 2 RAMB18	454.55 MHz
AMD® Zynq® MPSoC[‡]	1403 LUT, 2 RAMB18	457.67 MHz
Microchip® PolarFire® [§]	3546 4LUT, 4 LSRAM	230.10 MHz

Table 1: Resource usage and performance of XIP8001B on various FPGA families.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.
[§]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP8001B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP8001B with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (μm^2)	f_{target} [3]
7294	1891	400 MHz

Table 2: Logic requirements and performance of XIP8001B on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP8001B.

Type	Address depth	Data Width (bits)	Total (bits)
Single Port	256	32	8192
Single Port	128	32	4096
			12288

Table 3: Memory requirements of XIP8001B.

Throughput and Latency

The throughput and latency of the XIP8001B TRNG is independent of the main clock frequency as the internally (that is, inside the XIP8001B) generated independent clock frequency determines the throughput and latency.

However, in a correctly implemented TRNG the latency and throughput can be approximated as a function of the main clock frequency.

As an example, the startup time from releasing the reset and getting access to first 32-bit random word output is approximately 20k main clock cycles. Likewise the throughput in a typical correctly implemented TRNG is approximately one (1) bit per 40 main clock cycles.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.