PEACE OF MIND IN A DANGEROUS WORLD

XIP7410B: SECURE BOOT

A Quantum-Resistant nQrux® Secure Boot IP core

Resource Sheet

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sales@xiphera.com

Introduction

This document details FPGA and ASIC resource requirements and performance of XIP7410B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP7410B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$
Altera® Cyclone® 10 GX†	16586 ALM, 7 M20K, 2 DSP	163.75 MHz
Altera® Agilex® 5†	18291 ALM, 7 M20K, 2 DSP	166.36 MHz
AMD® Zynq® MPSoC‡	24109 LUT, 1/1 RAMB36/18, 3 DSP	305.25 MHz
AMD® Versal® Prime‡	25193 LUT, 1/1 RAMB36/18, 2 DSP	308.93 MHz
Lattice® CertusPro-NX® §	44082 LUT4, 16 EBR, 10/5 MULT9/MULT18	105.45 MHz
Lattice® Avant® §	44460 LUT4, 10 EBR, 3 MULT18	116.69 MHz
Microchip® PolarFire® ¶	50355 4LUT, 6/12 uSRAM/LSRAM, 5 Math	102.03 MHz

Table 1: Resource usage and performance of XIP7410B on various FPGA families.

†Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
‡Vivado 2024.2, default compilation settings, industrial speedgrade.
§Radiant 2025.1.0, default compilation settings, industrial speedgrade.
¶Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP7410B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP7410B with Synopsys® DC T-2022.03 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
165629	42931	1.0 GHz

Table 2: Logic requirements and performance of XIP7410B on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP7410B.

Type	Address depth	Data Width (bits)	Total (bits)
Single Port RAM	1024	16	16384
Single Port RAM	1024	16	16384
Single Port RAM	1024	64	65536
Simple Dual Port RAM	2048	23	47104
Simple Dual Port RAM	2048	23	47104
			159744

Table 3: Memory requirements of XIP7410B.

Throughput and Latency

All three operations, SHA-3 hash, and ECDSA and ML-DSA signature verification are performed in parallel in XIP7410B. Hence, the overall latency depends on the maximum latency of any of the three.

The overall latency is in practice determined only by ECDSA and SHA-3 computations. An ECDSA verification takes about 13,000,000 clock cycles. The SHA-3 computation starts dominating in the latency after the binary image size exceeds about 10–15 MB.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.