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XIP7213E: IPSEC AES-256-GCM

Extreme-Speed IPsec

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP7213E with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP7213E.

This document presents the resource usage information for 128-bit data width.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera® Agilex® 7 F[†]	23306 ALM, 62 M20K	343.88 MHz	44.02 Gbps
AMD® Versal® Prime[‡]	22725 LUT, 28 RAMB36	376.08 MHz	48.14 Gbps

Table 1: Resource usage and performance of XIP7213E on various FPGA families.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP7213E on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP7213E with Synopsys® DC W-2024.09-SP2 using default settings.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
135735	35183	667 MHz

Table 2: Logic requirements and performance of XIP7213E on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP7213E.

Type	Address depth	Data Width (bits)	Total (bits)
Simple Dual Port	7	128	8192
Simple Dual Port	5	256	8192
Simple Dual Port	5	64	8192
SPRAM	32	11	352
SPRAM	32	8	256
SPRAM	32	8	256
SPRAM	256	128	32768
True Dual Port	32	96	3072
True Dual Port	32	64	2048
True Dual Port	32	96	3072
True Dual Port	32	64	2048
16 RX SA rams			
True Dual Port	256	32	$8192 * 16$
			183136

Table 3: Memory requirements of XIP7213E.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.