PEACE OF MIND IN A DANGEROUS WORLD

XIP5012C: RSA SIGNATURE VERIFICATION

RSA Signature Verification IP Core

Resource Sheet

2026-05-06

sales@xiphera.com

Introduction

This document details FPGA and ASIC resource requirements and performance of XIP5012C with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP5012C.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP5012C on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP5012C with Synopsys® DC W-2024.09-SP2 using default settings.
Table 3 presents the total memories inside the XIP5012C.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
[‡]Quartus Prime Standard 24.1std.0, default compilation settings, industrial speedgrade.
[§]Vivado 2024.2, default compilation settings, industrial speedgrade.
[¶]Radiant 2024.2.1, default compilation settings, industrial speedgrade.
[‖]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.
[1]Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2]Excluding IO pins and memories listed in Table 3.
[3]Target frequency. Does not account for routing delays.

FPGA Family	Resources	$f_{\max}$
Altera® Agilex® 3 C†	251 ALM, 4 M20K	209.60 MHz
Altera® Cyclone® 10 GX†	265 ALM, 4 M20K	187.27 MHz
Altera® Cyclone® 10 LP‡	482 LE, 4 M9K	100.04 MHz
AMD® Zynq-7000® §	471 LUT, 1 RAMB36	146.05 MHz
AMD® Spartan-7® §	470 LUT, 1 RAMB36	170.79 MHz
Lattice® Avant® ¶	472 LUT4, 2 EBR	150.44 MHz
Lattice® CertusPro-NX® ¶	553 LUT4, 4 EBR	140.17 MHz
Microchip® PolarFire® ‖	677 4LUT, 4 LSRAM	181.69 MHz

Table 1: Resource usage and performance of XIP5012C on various FPGA families.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
1799	466	667 MHz

Table 2: Logic requirements and performance of XIP5012C on TSMC 16 nm FF+ process.

Type	Address depth	Data Width (bits)	Total (bits)
SPRAM	128	32	4096
SPRAM	128	32	4096
True Dual Port	512	32	16384
			24576

Table 3: Memory requirements of XIP5012C.