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XIP4003C: X25519 AND Ed25519

Curve25519 Key Exchange and Digital Signature IP Core

Resource Sheet

2026-05-06

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP4003C with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP4003C.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$
Altera® Cyclone® 10 GX†	481 ALM, 5 M20K, 1 DSP	258.26 MHz
Altera® Agilex® 3 C†	483 ALM, 5 M20K, 1 DSP	295.07 MHz
AMD® Zynq-7000® ‡	1040 LUT, 1/1 RAMB36/18, 1 DSP	178.00 MHz
AMD® Spartan-7® ‡	1034 LUT, 1/1 RAMB36/18, 1 DSP	201.13 MHz
Lattice® CertusPro-NX® §	1239 LUT4, 4 EBR, 2/1 MULT9/MULT18	170.27 MHz
Microchip® PolarFire® ¶	2960 4LUT, 1 LSRAM, 1 Math	229.57 MHz

Table 1: Resource usage and performance of XIP4003C on various FPGA families.

†Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
‡Vivado 2024.2, default compilation settings, industrial speedgrade.
§Radiant 2024.2.1, default compilation settings, industrial speedgrade.
¶Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP4003C on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP4003C with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
6267	1624	667 MHz

Table 2: Logic requirements and performance of XIP4003C on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP4003C.

Type	Address depth	Data Width (bits)	Total (bits)
ROM	1024	22	22528
ROM	2048	15	30720
Simple Dual Port	688	18	12384
			65632

Table 3: Memory requirements of XIP4003C.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.