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XIP3327C: HKDF/HMAC/SHA-256/SHA-512 SHA-256 IP Core with Extended Functionalities

Resource Sheet

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Introduction

This document details FPGA resource requirements and performance of XIP3327C with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP3327C.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Quartus Prime Standard 24.1std.0, default compilation settings, industrial speedgrade.

[§]Vivado 2024.2, default compilation settings, industrial speedgrade.

[¶]Radiant 2024.2.1, default compilation settings, industrial speedgrade.

^{||}Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

FPGA Family	Resources	f_{max}
Altera® Agilex® 3 C [†]	993 ALM, 7 M20K	228.15 MHz
Altera® Cyclone® 10 GX [†]	1030 ALM, 7 M20K	184.50 MHz
Altera® Cyclone® 10 LP [†]	2616 LE, 5 M9K	117.43 MHz
AMD® Spartan-7® §	1137 LUT, 2/1 RAMB36/18	176.06 MHz
AMD® Zynq-7000® §	1160 LUT, 2/1 RAMB36/18	161.37 MHz
Lattice® CertusPro-NX® ¶	2499 LUT4, 4 EBR	117.07 MHz
Lattice® Avant® ¶	4890 LUT4, 2 EBR	131.32 MHz
Microchip® PolarFire®	3097 4LUT, 3/6 uSRAM/LSRAM	177.68 MHz

Table 1: Resource usage and performance of XIP3327C on various FPGA families.