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XIP3323B: HKDF/HMAC/SHA-384

SHA-384 IP Core with Extended Functionalities

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP3323B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP3323B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$
Altera® Cyclone® 10 GX†	2519 ALM, 6 M20K	190.51 MHz
Altera® Agilex® 5†	2609 ALM, 6 M20K	149.39 MHz
AMD® Versal® Prime‡	3432 LUT, 2 RAMB36	362.19 MHz
AMD® Zynq® MPSoC‡	2684 LUT, 2 RAMB36	286.12 MHz
Lattice® CertusPro-NX® §	5970 LUT4, 6 EBR	90.12 MHz
Lattice® Avant® §	6214 LUT4, 2 EBR	103.63 MHz
Microchip® PolarFire® ¶	5100 4LUT, 6/8 uSRAM/LSRAM	164.15 MHz

Table 1: Resource usage and performance of XIP3323B on various FPGA families.

†Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
‡Vivado 2024.2, default compilation settings, industrial speedgrade.
§Radiant 2024.2.1, default compilation settings, industrial speedgrade.
¶Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP3323B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP3323B with Synopsys® DC T-2022.03 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (μm^2)	f_{target} [3]
26247	6803	750 MHz

Table 2: Logic requirements and performance of XIP3323B on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP3323B.

Type	Address depth	Data Width (bits)	Total (bits)
Simple Dual Port	18	65	1170
Simple Dual Port	32	68	2176
			3346

Table 3: Memory requirements of XIP3323B.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.