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XIP3030H: SHA-3

A High-Speed Versatile Core for SHA-3-224/256/384/512 and (c)SHAKE-128/256

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP3030H with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP3030H.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP3030H on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP3030H with Synopsys[®] DC T-2022.03 using default settings.

The XIP3030H does not contain any internal memories.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.

[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.

[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

¹Equivalent to the total cell area normalised to the area of a representative NAND2 gate.

²Excluding IO pins.

³Target frequency. Does not account for routing delays.

| FPGA Family | Resources | f_{\max} | Throughput |
|-------------------------------------|------------|------------|------------|
| Altera® Cyclone® 10 GX [†] | 3539 ALM | 310.85 MHz | 19.89 Gbps |
| Altera® Agilex® 7 F [†] | 3539 ALM | 310.85 MHz | 19.89 Gbps |
| AMD® Versal® Prime [‡] | 5918 LUT | 515.20 MHz | 32.97 Gbps |
| AMD® Zynq® MPSoC [‡] | 6330 LUT | 602.41 MHz | 38.55 Gbps |
| Lattice® CertusPro-NX [§] | 12018 LUT4 | 145.56 MHz | 9.32 Gbps |
| Lattice® Avant [§] | 11787 LUT4 | 207.81 MHz | 13.30 Gbps |
| Microchip® PolarFire® [¶] | 13114 4LUT | 217.91 MHz | 13.95 Gbps |

Table 1: Resource usage and performance of XIP3030H on various FPGA families.

| Total Gate Equivalent ¹ | Total Cell Area ² (μm^2) | f_{target} ³ |
|------------------------------------|--|----------------------------------|
| 37104 | 9617 | 1.0 GHz |

Table 2: Logic requirements and performance of XIP3030H on TSMC 16 nm FF+ process.