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XIP3030C: SHA-3

A Compact Versatile Core for SHA-3-224/256/384/512 and (c)SHAKE-128/256

Resource Sheet

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sales@xiphera.com

Introduction

This document details FPGA and ASIC resource requirements and performance of XIP3030C with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP3030C.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP3030C on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP3030C with Synopsys® DC T-2022.03 using default settings.
Table 3 presents the total memories inside the XIP3030C.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.
[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.
[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.
[1]Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2]Excluding IO pins and memories listed in Table 3.
[3]Target frequency. Does not account for routing delays.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera® Agilex® 3 C†	662 ALM, 3 M20K	248.02 MHz	112.76 Mbps
Altera® Cyclone® 10 GX†	732 ALM, 3 M20K	212.31 MHz	96.53 Mbps
AMD® Spartan-7® ‡	824 LUT, 1/1 RAMB36/18	174.31 MHz	79.25 Mbps
AMD® Zynq-7000® ‡	836 LUT, 1/1 RAMB36/18	153.56 MHz	69.82 Mbps
Lattice® Avant® §	1357 LUT4, 2 EBR	187.94 MHz	85.45 Mbps
Lattice® CertusPro-NX® §	1225 LUT4, 3 EBR	158.91 MHz	72.25 Mbps
Microchip® PolarFire® ¶	2183 4LUT, 2 LSRAM	174.40 MHz	79.29 Mbps

Table 1: Resource usage and performance of XIP3030C on various FPGA families.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
4211	1091	400 MHz

Table 2: Logic requirements and performance of XIP3030C on TSMC 16 nm FF+ process.

Type	Address depth	Data Width (bits)	Total (bits)
ROM	256	19	4864
SDPRAM	128	64	8192
			13056

Table 3: Memory requirements of XIP3030C.