



PEACE OF MIND IN A DANGEROUS WORLD

XIP2201B: ASCON

A Lightweight Cryptographic Suite for AEAD and Hashing

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP2201B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP2201B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP2201B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP2201B with Synopsys[®] DC W-2024.09-SP2 using default settings.

The XIP2201B does not contain any internal memories.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.

[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.

[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

¹Equivalent to the total cell area normalised to the area of a representative NAND2 gate.

²Excluding IO pins.

³Target frequency. Does not account for routing delays.

FPGA Family	Resources	f_{\max}	Throughput
Altera® Agilex® 5 [†]	1895 ALM	392.00 MHz	1.93 Gbps
Altera® Cyclone® 10 GX [†]	1817 ALM	423.01 MHz	2.08 Gbps
AMD® Versal® Prime [‡]	2484 LUT	435.73 MHz	2.15 Gbps
AMD® Zynq® MPSoC [‡]	2325 LUT	430.11 MHz	2.12 Gbps
Lattice® Avant® [§]	4922 LUT4	307.50 MHz	1.51 Gbps
Lattice® CertusPro-NX® [§]	4730 LUT4	156.20 MHz	768.99 Mbps
Microchip® PolarFire® [¶]	5417 4LUT	255.30 MHz	1.26 Gbps

Table 1: Resource usage and performance of XIP2201B on various FPGA families.

Total Gate Equivalent ¹	Total Cell Area ² (μm^2)	f_{target} ³
15486	4014	1.0 GHz

Table 2: Logic requirements and performance of XIP2201B on TSMC 16 nm FF+ process.

Throughput and Latency

The maximum throughput in the Table 1 is calculated with the Equation 1. This is the throughput for the Ascon-AEAD128 mode. This means that with long packets the effective latency for one block of data is 13 clock cycles.

$$\text{Throughput} = \frac{64\text{bits}}{13 \text{ clock cycles}} * f_{\text{MAX}} \quad (1)$$