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XIP2113B: CHACHA20-POLY1305

Balanced IP Core for ChaCha20-Poly1305 Authenticated Encryption

Resource Sheet

2026-05-06

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP2113B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP2113B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	f_{\max}	Throughput
Altera® Cyclone® 10 GX [†]	5288 ALM, 8 M20K, 36 DSP	116.50 MHz	2.71 Gbps
Altera® Agilex® 5 [†]	5586 ALM, 8 M20K, 36 DSP	105.27 MHz	2.45 Gbps
AMD® Versal® Prime [‡]	8575 LUT , 36 DSP	372.44 MHz	8.67 Gbps
AMD® Zynq® MPSoC [‡]	7332 LUT , 72 DSP	309.31 MHz	7.20 Gbps
Lattice® Avant® [§]	15257 LUT4 , 66 MULT18	121.34 MHz	2.82 Gbps
Lattice® CertusPro-NX® [§]	15650 LUT4, 8 EBR, 242/121 MULT9/MULT18	84.87 MHz	1.98 Gbps
Microchip® PolarFire® [¶]	17146 4LUT, 24 uSRAM, 121 Math	147.86 MHz	3.44 Gbps

Table 1: Resource usage and performance of XIP2113B on various FPGA families.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.

[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.

[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP2113B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP2113B with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent ¹	Total Cell Area ² (μm^2)	f_{target} ³
159560	41358	1.0 GHz

Table 2: Logic requirements and performance of XIP2113B on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP2113B.

Type	Address depth	Data Width (bits)	Total (bits)
SPRAM	16	134	2144
SPRAM	16	134	2144
			4288

Table 3: Memory requirements of XIP2113B.

¹Equivalent to the total cell area normalised to the area of a representative NAND2 gate.

²Excluding IO pins and memories listed in Table 3.

³Target frequency. Does not account for routing delays.