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XIP1213H: MACSEC AES256-GCM

MACsec (IEEE 802.1AE) IP Core

Resource Sheet

2026-05-06

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1213H with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1213H.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera® Cyclone® 10 GX†	42237 ALM, 158 M20K	202.72 MHz	25.95 Gbps
Altera® Agilex® 7 F†	52621 ALM, 158 M20K	345.90 MHz	44.28 Gbps
AMD® Zynq® MPSoC‡	42611 LUT, 4/276 RAMB36/18	257.47 MHz	32.96 Gbps
AMD® Versal® Prime‡	34013 LUT, 4/276 RAMB36/18	323.31 MHz	41.38 Gbps
Lattice® Avant® §	62210 LUT4, 556 EBR	79.68 MHz	10.20 Gbps
Lattice® CertusPro-NX® §	144801 LUT4, 556 EBR	79.68 MHz	10.20 Gbps
Microchip® PolarFire® ¶	115463 4LUT, 95/51 uSRAM/LSRAM	144.43 MHz	18.49 Gbps

Table 1: Resource usage and performance of XIP1213H on various FPGA families.

†Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
‡Vivado 2024.2, default compilation settings, industrial speedgrade.
§Radiant 2024.2.1, default compilation settings, industrial speedgrade.
¶Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1213H on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1213H with Synopsys® DC T-2022.03 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (μm^2)	f_{target} [3]
529573	137265	400 MHz

Table 2: Logic requirements and performance of XIP1213H on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP1213H. Memory usage can vary with implementation options.

Type	Address depth	Data Width (bits)	Total (bits)
Simple Dual Port	16	256	4096
Simple Dual Port	16	15	240
Simple Dual Port	16	128	2048
Simple Dual Port	16	32	512
Simple Dual Port	16	15	240
Simple Dual Port	16	32	512
			7648

Table 3: Memory requirements of XIP1213H.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.