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XIP1213E: MACSEC AES256-GCM

Extreme Speed MACsec (IEEE 802.1AE) IP Core

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1213E with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1213E.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

The throughput in Table 1 is achieved by multiplying the datapath width with $F_{\max}$, and it applies for long packets. The different variants marked as *-128* presents the different datapath width options.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1213E on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1213E with Synopsys® DC W-2024.09-SP2 using default settings.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.
[§]Radiant 2025.1.0, default compilation settings, industrial speedgrade.
[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.
[1]Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2]Excluding IO pins.
[3]Target frequency. Does not account for routing delays.

FPGA Family	Resources	f_{max}	Throughput
XIP1213E-128			
Altera® Agilex® 7 F†	66749 ALM, 28 M20K	437.83 MHz	56.04 Gbps
AMD® Versal® Prime‡	60037 LUT, 28/2 RAMB36/18	402.74 MHz	51.55 Gbps
Lattice® Avant® §	142517 LUT4	117.91 MHz	15.09 Gbps
Microchip® PolarFire® ¶	115429 4LUT, 95/51 uSRAM/LSRAM	139.96 MHz	17.91 Gbps
XIP1213E-256			
Altera® Agilex® 7 F†	106750 ALM, 28 M20K	454.13 MHz	116.26 Gbps
AMD® Versal® Prime‡	106132 LUT, 28/2 RAMB36/18	400.16 MHz	102.44 Gbps
Lattice® Avant® §	231848 LUT4	104.87 MHz	26.85 Gbps
XIP1213E-512			
Altera® Agilex® 7 F†	189918 ALM, 28 M20K	435.35 MHz	222.90 Gbps
AMD® Versal® Prime‡	193781 LUT, 28/2 RAMB36/18	348.55 MHz	178.46 Gbps
Microchip® PolarFire® ¶	380867 4LUT, 83/55 uSRAM/LSRAM	126.10 MHz	64.56 Gbps
XIP1213E-1024			
Altera® Agilex® 7 F†	337050 ALM, 28 M20K	398.57 MHz	408.14 Gbps
AMD® Versal® Prime‡	355907 LUT, 28/2 RAMB36/18	344.00 MHz	352.25 Gbps

Table 1: Resource usage and performance of XIP1213E on various FPGA families.

Core version	Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
XIP1213E-128	584609	151531	667 MHz
XIP1213E-256	1027912	266435	667 MHz
XIP1213E-512	1828197	473869	667 MHz
XIP1213E-1024	3346996	867541	667 MHz

Table 2: Logic requirements and performance of XIP1213E on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP1213E. Memory usage can vary with implementation options.

Type	Address depth	Data Width (bits)	Total (bits)
Simple Dual Port	16	256	4096
Simple Dual Port	16	15	240
Simple Dual Port	16	128	2048
Simple Dual Port	16	32	512
Simple Dual Port	16	15	240
Simple Dual Port	16	32	512
			7648

Table 3: Memory requirements of XIP1213E.

Throughput and Latency

Table 4 presents latency of IP with different data widths on receive and transmit directions. Idle column indicates number of cycles between frames when IP keeps ready low. Depeding of bus width different number of cycles is needed on transmit side to compensate maximum number of added bytes on output. On RX one cycle is need for AESGCM key expansion.

Bus width	Direction	Cycles	Idle Cycles
128-bit	Transmit	39	5
256-bit	Transmit	41	2
512-bit	Transmit	42	2
1024-bit	Transmit	42	2
128-bit	Receive	43	1
256-bit	Receive	43	1
512-bit	Receive	43	1
1024-bit	Receive	43	1

Table 4: Latency from start of packet in to start of packet out as linerate clock cycles.