PEACE OF MIND IN A DANGEROUS WORLD

XIP1213B: MACSEC AES256-GCM

MACsec (IEEE 802.1AE) IP Core

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1213B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1213B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera® Cyclone® 10 GX†	9857 ALM, 46 M20K	227.74 MHz	2.08 Gbps
Altera® Agilex® 5†	11381 ALM, 46 M20K	224.06 MHz	2.05 Gbps
AMD® Zynq® MPSoC‡	14251 LUT, 4 RAMB36	311.14 MHz	2.84 Gbps
AMD® Versal® Prime‡	14352 LUT, 4 RAMB36	378.21 MHz	3.46 Gbps
Lattice® CertusPro-NX® §	24054 LUT4, 50 EBR	110.08 MHz	1.01 Gbps
Lattice® Avant® §	26638 LUT4, 4 EBR	161.58 MHz	1.48 Gbps
Microchip® PolarFire® ¶	32793 4LUT, 122/8 uSRAM/LSRAM	193.69 MHz	1.77 Gbps

Table 1: Resource usage and performance of XIP1213B on various FPGA families.

†Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
‡Vivado 2024.2, default compilation settings, industrial speedgrade.
§Radiant 2024.2.1, default compilation settings, industrial speedgrade.
¶Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1213B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1213B with Synopsys® DC T-2022.03 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
109169	28297	320 MHz

Table 2: Logic requirements and performance of XIP1213B on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP1213B.

Type	Address depth	Data Width (bits)	Total (bits)
Simple Dual Port	16	256	4096
			4096

Table 3: Memory requirements of XIP1213B.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.