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XIP1183H: AES256-XTS

Advanced Encryption Standard (256-bit key), XTS mode IP Core

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1183H with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1183H.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	f_{\max}	Throughput
Altera® Agilex® 7 F [†]	28529 ALM, 4 M20K	397.46 MHz	50.87 Gbps
Altera® Cyclone® 10 GX [†]	28861 ALM, 4 M20K	230.95 MHz	29.56 Gbps
AMD® Zynq® MPSoC [‡]	33361 LUT	328.73 MHz	42.08 Gbps
AMD® Versal® Prime [‡]	33914 LUT	334.67 MHz	42.84 Gbps
Lattice® Avant® [§]	125059 LUT4, 2 EBR	110.68 MHz	14.17 Gbps
Microchip® PolarFire® [¶]	152219 4LUT, 11 uSRAM	109.48 MHz	14.01 Gbps

Table 1: Resource usage and performance of XIP1183H on various FPGA families.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.

[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.

[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1183H on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1183H with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent ¹	Total Cell Area ² (μm ²)	f_{target} ³
240770	62408	667 MHz

Table 2: Logic requirements and performance of XIP1183H on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP1183H.

Type	Address depth	Data Width (bits)	Total (bits)
True dual port RAM	16	128	2048
			2048

Table 3: Memory requirements of XIP1183H.

¹Equivalent to the total cell area normalised to the area of a representative NAND2 gate.

²Excluding IO pins and memories listed in Table 3.

³Target frequency. Does not account for routing delays.