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XIP1183B: AES256-XTS

Advanced Encryption Standard (256-bit key), XTS mode IP Core

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1183B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1183B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera® Agilex® 5[†]	6021 ALM, 8 M20K	213.81 MHz	1.71 Gbps
Altera® Cyclone® 10 GX[†]	6050 ALM, 8 M20K	251.57 MHz	2.01 Gbps
AMD® Versal® Prime[‡]	6612 LUT	346.86 MHz	2.77 Gbps
AMD® Zynq® MPSoC[‡]	7029 LUT	360.88 MHz	2.89 Gbps
Lattice® Avant® [§]	20816 LUT4, 4 EBR	129.75 MHz	1.04 Gbps
Lattice® CertusPro-NX® [§]	19948 LUT4, 8 EBR	110.62 MHz	884.95 Mbps
Microchip® PolarFire® [¶]	26637 4LUT, 22 uSRAM	140.51 MHz	1.12 Gbps

Table 1: Resource usage and performance of XIP1183B on various FPGA families.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.
[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.
[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1183B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1183B with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
43650	11314	667 MHz

Table 2: Logic requirements and performance of XIP1183B on TSMC 16 nm FF+ process.

Table 3 presents the total memories inside the XIP1183B.

Type	Address depth	Data Width (bits)	Total (bits)
SPRAM	16	128	2048
SPRAM	16	128	2048
			4096

Table 3: Memory requirements of XIP1183B.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table 3.
[3] Target frequency. Does not account for routing delays.