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XIP1123B: VERSATILE AES-256 IP CORE

Advanced Encryption Standard (256-bit key), ECB, CBC, OFB, CFB, and CTR Mode of Operation

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1123B with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1123B.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1123B on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1123B with Synopsys[®] DC T-2022.03 using default settings.

Table 3 presents the total memories inside the XIP1123B.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.

[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.

[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

¹Equivalent to the total cell area normalised to the area of a representative NAND2 gate.

²Excluding IO pins and memories listed in Table 3.

³Target frequency. Does not account for routing delays.

FPGA Family	Resources	f_{\max}	Throughput
Altera® Agilex® 5 [†]	3659 ALM, 4 M20K	216.73 MHz	1.73 Gbps
Altera® Cyclone® 10 GX [†]	3786 ALM, 4 M20K	243.31 MHz	1.95 Gbps
AMD® Versal® Prime [‡]	4395 LUT	342.35 MHz	2.74 Gbps
AMD® Zynq® MPSoC [‡]	4461 LUT	362.58 MHz	2.90 Gbps
Lattice® CertusPro-NX® [§]	4216 LUT4, 28 EBR	166.61 MHz	1.33 Gbps
Lattice® Avant® [§]	4375 LUT4, 26 EBR	196.50 MHz	1.57 Gbps
Microchip® PolarFire® [¶]	16596 4LUT, 11 uSRAM	136.54 MHz	1.09 Gbps

Table 1: Resource usage and performance of XIP1123B on various FPGA families.

Total Gate Equivalent ¹	Total Cell Area ² (μm^2)	f_{target} ³
25818	6692	750 MHz

Table 2: Logic requirements and performance of XIP1123B on TSMC 16 nm FF+ process.

Type	Address depth	Data Width (bits)	Total (bits)
Simple Dual Port	16	128	2048
			2048

Table 3: Memory requirements of XIP1123B.