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XIP1113H: AES128/192/256-GCM

Advanced Encryption Standard, Galois Counter Mode IP Core

Resource Sheet

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1113H with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1113H.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1113H on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1113H with Synopsys[®] DC T-2022.03 using default settings.

The XIP1113H does not contain any internal memories.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.

[§]Radiant 2024.2.1, default compilation settings, industrial speedgrade.

[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

¹Equivalent to the total cell area normalised to the area of a representative NAND2 gate.

²Excluding IO pins.

³Target frequency. Does not account for routing delays.

| FPGA Family | Resources | f_{\max} | Throughput |
|-------------------------------------|-------------------|------------|------------|
| Altera® Agilex® 7 F [†] | 25910 ALM | 554.94 MHz | 71.03 Gbps |
| Altera® Cyclone® 10 GX [†] | 23666 ALM | 319.18 MHz | 40.86 Gbps |
| AMD® Zynq® MPSoC [‡] | 30012 LUT | 389.41 MHz | 49.84 Gbps |
| AMD® Versal® Prime [†] | 29322 LUT | 447.43 MHz | 57.27 Gbps |
| Lattice® CertusPro-NX [§] | 49682 LUT4, 8 EBR | 103.72 MHz | 13.28 Gbps |
| Lattice® Avant [§] | 53990 LUT4 | 117.36 MHz | 15.02 Gbps |
| Microchip® PolarFire® ¶ | 50628 4LUT | 141.16 MHz | 18.07 Gbps |

Table 1: Resource usage and performance of XIP1113H on various FPGA families.

| Total Gate Equivalent ¹ | Total Cell Area ² (μm^2) | f_{target} ³ |
|------------------------------------|--|----------------------------------|
| 155343 | 40265 | 870 MHz |

Table 2: Logic requirements and performance of XIP1113H on TSMC 16 nm FF+ process.