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XIP1113E: AES128/192/256-GCM

Extreme Speed IP Cores for AES-GCM Authenticated Encryption

Resource Sheet

2026-05-06

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Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1113E with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1113E.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

The throughput in Table 1 is achieved by multiplying the datapath width with F_{max}, and it applies for long packets. The different variants marked as *-128* presents the different datapath width options.

ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1113E on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1113E with Synopsys® DC T-2022.03 using default settings.

[†]Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.
[‡]Vivado 2024.2, default compilation settings, industrial speedgrade.
[§]Radiant 2025.1.0, default compilation settings, industrial speedgrade.
[¶]Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

FPGA Family	Resources	$f_{\max}$	Throughput
XIP1113E-128			
Altera® Agilex® 7 F†	24854 ALM	523.83 MHz	67.05 Gbps
AMD® Versal® Prime‡	26645 LUT	402.90 MHz	51.57 Gbps
Lattice® Avant® §	53970 LUT4	121.88 MHz	15.60 Gbps
Microchip® PolarFire® ¶	50596 4LUT	133.05 MHz	17.03 Gbps
XIP1113E-256			
Altera® Agilex® 7 F†	43495 ALM	506.07 MHz	129.55 Gbps
AMD® Versal® Prime‡	47724 LUT	400.00 MHz	102.40 Gbps
Lattice® Avant® §	97599 LUT4	112.45 MHz	28.79 Gbps
Microchip® PolarFire® ¶	89308 4LUT	133.30 MHz	34.12 Gbps
XIP1113E-512			
Altera® Agilex® 7 F†	80384 ALM	484.50 MHz	248.06 Gbps
AMD® Versal® Prime‡	89383 LUT	400.00 MHz	204.80 Gbps
Lattice® Avant® §	183653 LUT4	102.11 MHz	52.28 Gbps
Microchip® PolarFire® ¶	171413 4LUT	125.14 MHz	64.07 Gbps
XIP1113E-1024			
Altera® Agilex® 7 F†	152484 ALM	476.64 MHz	488.08 Gbps
AMD® Versal® Prime‡	163121 LUT	392.46 MHz	401.88 Gbps
Microchip® PolarFire® ¶	322921 4LUT	115.45 MHz	118.22 Gbps

Table 1: Resource usage and performance of XIP1113E on various FPGA families.

Core version	Total Gate Equivalent [1]	Total Cell Area [2] (µm²)	f_{target} [3]
XIP1113E-128	267256	69273	870 MHz
XIP1113E-256	460414	119339	800 MHz
XIP1113E-512	837953	217197	800 MHz
XIP1113E-1024	1544708	400388	769 MHz

Table 2: Logic requirements and performance of XIP1113E on TSMC 16 nm FF+ process.

The XIP1113E does not contain any internal memories.

Throughput and Latency

Performance of XIP1113E is determined by the ability to start new message processing in the core because XIP1113E all input words are written in consecutive clock periods after the processing has started and all input words are processed with a constant latency of L clock cycles (see Table 3). The latency is measured from rising edge of `new_msg_i` to rising edge of `data_valid_o`. With 128-bit databus there needs to be always one cycle pause between frames.

[1] Equivalent to the total cell area normalised to the area of a representative NAND2 gate.
[2] Excluding IO pins and memories listed in Table **??**.
[3] Target frequency. Does not account for routing delays.

Version	L
XIP1113E 128-bit	28
XIP1113E 256-bit	30
XIP1113E 512-bit	31
XIP1113E 1024-bit	31

Table 3: Latencies of XIP1113E versions