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XIP1113B: AES256-GCM

Advanced Encryption Standard (256-bit key), Galois Counter Mode IP Core

Product Brief
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Introduction

XIP1113B from Xiphera is a balanced Intellectual Property (IP) core implementing the Advanced Encryption Standard (AES) [2] in Galois Counter Mode (GCM) [3]. AES-GCM is a widely used cryptographic algorithm for Authenticated Enryption with Associated Data (AEAD) purposes, as it provides both data confidentiality and authenticity.

XIP1113B has been designed for easy integration with FPGA- and ASIC-based designs in a vendor-agnostic design methodology, and the functionality of XIP1113B does not rely on any FPGA manufacturer-specific features.

Key Features

- **Compact** resource requirements: The entire XIP1113B requires 2902 Adaptive Lookup Modules (ALMs) (Intel® Arria® 10 GX), and does not require any multipliers, DSPBlocks or internal memory[1] in a typical FPGA implementation.
- **Performance:** Despite its compact size, XIP1113B achieves a throughput in the Gbps range[2], for example 4.00+ Gbps in Xilinx® Zynq® MPSoC.
- **Standard Compliance:** XIP1113B is fully compliant with both the Advanced Encryption Algorithm (AES) standard [2], as well as with the Galois Counter Mode (GCM) standard [3].
- **Test Vector Compliance:** XIP1113B passes all test vectors specified in [1].

[1]The parameterizable input and output FIFOs may optionally be instantiated with internal memory blocks, but the actual XIP1113B kernel requires only logic resources.

[2]As is typical for AEAD algorithms, the highest throughput is achieved for long messages.

- 32-bit FIFO Interfaces[3] ease the integration of XIP1113B with other FPGA logic and/or control software.

Functionality

The main functionality of XIP1113B depends on the mode of operation. When XIP1113B operates in the encryption and authentication tag calculation mode, it encrypts the incoming plaintext blocks into ciphertext blocks, and in addition to this also calculates a 128 bits long authentication tag from both the incoming plaintext and associated data. When XIP1113B operates in the decryption and tag validity cheching mode, it decrypts the incoming ciphertext blocks into plaintext blocks, and validates the received authentication tag value by calculating the tag from the incoming ciphertext and associated data blocks and comparing the resulting tag value with the received tag value. As defined by the GCM mode of operation, associated data is included in the authentication tag calculation.

XIP1113B can also operate with zero-length associated data, meaning that XIP1113B treats all signals on the input `data_in` as plaintext to be encrypted or as ciphertext to be decrypted. XIP1113B can also operate with zero-length plaintext or ciphertext, in which case it acts only as an authenticator or authentication validity checker.

XIP1113B outputs first the associated data, followed by encrypted plaintext or decrypted ciphertext (depending on the mode of operation), and as the last output the tag value and associated status signals.

Block Diagram

The internal high-level block diagram of XIP1113B is depicted in Figure 1.

Interfaces

The external interfaces of XIP1113B are depicted in Figure 2.

This Product Brief describes a high-level overview of the functionality and capabilities of XIP1113B. Please contact sales@xiphera.com for a complete datasheet with a detailed description of the input and output signals, startup procedure of XIP1113B, example simulation waveforms, and the FPGA resource requirements of your targeted FPGA family.

FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for representative implementations on two different FPGA architectures. On request, the resource estimates can also be supplied for other FPGA families.

[3] XIP1113B is also available with 128-bits long interfaces, please contact sales@xiphera.com for details.

[*] $Throughput = \frac{f_{MAX} * 128\ bits}{14\ clock\ cycles}$; achieved asymptotically with long packets.

[†] Quartus® Prime Pro 21.1.0, default compilation settings, industrial speedgrade.

[‡] Vivado 2020.2, default compilation settings, industrial speedgrade.

[§] Radiant 2022.1.0, default compilation settings, synthesised with Synplify.

[¶] Diamond 3.12.0, default compilation settings, synthesised with Synplify.

[‖] Libero 2022.1.0.10, default compilation settings, industrial speedgrade.

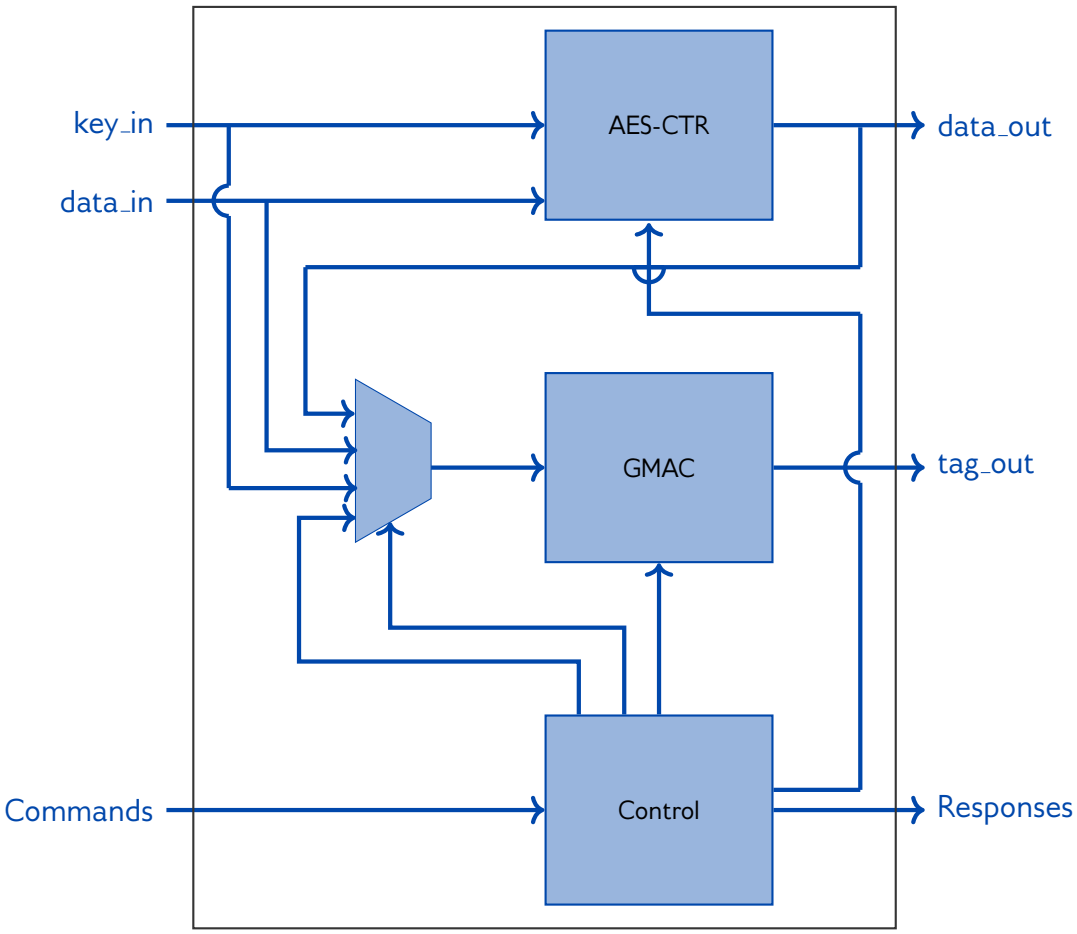

Figure 1: Internal high-level block diagram of XIP1113B

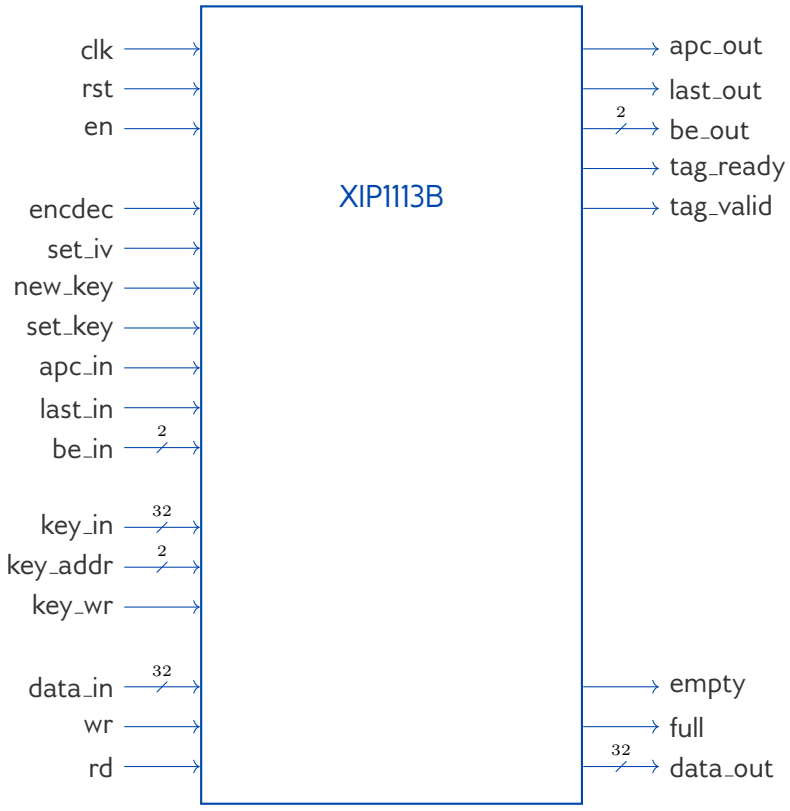

Figure 2: External interfaces of XIP1113B

Device	Resources	f_{MAX}	Max. throughput*
Intel® Arria® 10 GX†	2902 ALM	401.12 MHz	3.67 Gbps
Intel® Cyclone® 10 GX†	2895 ALM	381.53 MHz	3.49 Gbps
Xilinx® Zynq® MPSoC‡	3028 LUT	437.83 MHz	4.00 Gbps
Xilinx® Kintex® UltraScale+‡	3023 LUT	469.48 MHz	4.29 Gbps
Xilinx® Zynq-7000® ‡	3332 LUT	260.28 MHz	2.38 Gbps
Lattice® CrossLink-NX® §	4467 LUT4, 16 EBR	178.51 MHz	1.63 Gbps
Lattice® CertusPro-NX® §	5812 LUT4	155.13 MHz	1.42 Gbps
Lattice® ECP5® ¶	6134 LUT4	117.69 MHz	1.08 Gbps
Microchip® PolarFire® ‖	6019 4LUT	120.53 MHz	1.10 Gbps

Table 1: Resource usage and performance of XIP1113B on representative FPGA families.

Example Use Cases

XIP1113B has several applications, as AES-GCM is a popular AEAD algorithm in a number of standardized communications protocols, including IPSEC, MACSEC and TLS (Transport Layer Security) versions 1.2 and 1.3. Additionally, AES-GCM is used in fibre channel communications and tape storage applications.

Ordering and Deliverables

Please contact sales@xiphera.com for pricing and your preferred delivery method. XIP1113B can be shipped in a number of formats, including netlist, source code, or encrypted source code.

Additionally, synthesis scripts, a comprehensive testbench, and a detailed datasheet including an integration guide are included.

Export Control

XIP1113B protects data confidentiality and is a dual-use product as defined in the Wassenaar Arrangement. Consequently, the export of XIP1113B is controlled by Council Regulation (EC) No 428/2009 of 5 May 2009 and its subsequent changes.

XIP1113B can be immediately shipped to all European Union member states, Australia, Canada, Japan, New Zealand, Norway, Switzerland, United Kingdom, and the United States.

Export to other countries requires authorization from The Ministry for Foreign Affairs of Finland, and a typical processing time for an export authorization is a few weeks.

About Xiphera

Xiphera specializes in secure and efficient implementations of standardized cryptographic algorithms on Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs). Our fully in-house designed product portfolio includes individual cryptographic Intellectual Property (IP) cores, as well as comprehensive security solutions built from a combination of individual IP cores.

Xiphera is a Finnish company operating under the laws of the Republic of Finland, and is fully owned by Finnish citizens and institutional investors.

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References

[1] MACsec GCM-AES Test Vectors. `http://www.ieee802.org/1/files/public/docs2011/bn-randall-test-vectors-0511-v1.pdf`.

[2] Specification for the Advanced Encryption Standard (AES). Federal Information Processing Standards Publication 197, 2001.

[3] Morris J. Dworkin. SP 800-38D. Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC. Technical report, Gaithersburg, MD, United States, 2007.