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# XIP1103H: AES256-CTR

## High-speed IP Core for AES Counter Mode

Resource Sheet  
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### Introduction

This document details FPGA and ASIC resource requirements and performance of XIP1103H with the default configuration—for example, instantiation parameters, supported features, and selected bus interface—of XIP1103H.

### FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for different FPGA architectures. Upon request, resource requirements can also be provided for other FPGA manufacturers, families, and specific part numbers. The results were obtained using default synthesis and P&R (placement and routing) settings in the FPGA design software.

FPGA Family	Resources	$f_{\max}$	Throughput
Altera <sup>®</sup> Agilex <sup>®</sup> 7 F <sup>†</sup>	17014 ALM	720.46 MHz	92.22 Gbps
Altera <sup>®</sup> Cyclone <sup>®</sup> 10 GX <sup>‡</sup>	13689 ALM	510.99 MHz	65.41 Gbps
AMD <sup>®</sup> Zynq <sup>®</sup> MPSoC <sup>‡</sup>	15430 LUT	799.36 MHz	102.32 Gbps
AMD <sup>®</sup> Versal <sup>®</sup> Prime <sup>‡</sup>	15056 LUT	728.33 MHz	93.23 Gbps
Lattice <sup>®</sup> Avant <sup>®</sup> <sup>§</sup>	31791 LUT4	259.54 MHz	33.22 Gbps
Lattice <sup>®</sup> CertusPro-NX <sup>®</sup> <sup>§</sup>	29089 LUT4	214.32 MHz	27.43 Gbps
Microchip <sup>®</sup> PolarFire <sup>®</sup> <sup>¶</sup>	29828 4LUT, 12 uSRAM	275.86 MHz	35.31 Gbps

Table 1: Resource usage and performance of XIP1103H on various FPGA families.

<sup>†</sup>Quartus Prime Pro 25.1.0, default compilation settings, industrial speedgrade.

<sup>‡</sup>Vivado 2024.2, default compilation settings, industrial speedgrade.

<sup>§</sup>Radiant 2024.2.1, default compilation settings, industrial speedgrade.

<sup>¶</sup>Libero 2024.2.0.13, default compilation settings, industrial speedgrade.

## ASIC Resources and Performance

Table 2 describes the logic requirements of XIP1103H on the TSMC 16nm FinFET Plus Low Leakage standard cell process. The results were obtained by synthesising XIP1103H with Synopsys® DC W-2024.09-SP2 using default settings.

Total Gate Equivalent <sup>1</sup>	Total Cell Area <sup>2</sup> (μm <sup>2</sup> )	$f_{\text{target}}$ <sup>3</sup>
206513	53528	1.0 GHz

Table 2: Logic requirements and performance of XIP1103H on TSMC 16 nm FF+ process.

The XIP1103H does not contain any internal memories.

<sup>1</sup>Equivalent to the total cell area normalised to the area of a representative NAND2 gate.

<sup>2</sup>Excluding IO pins.

<sup>3</sup>Target frequency. Does not account for routing delays.