



# XIP1111H: AES128-GCM

## Advanced Encryption Standard (128-bit key), Galois Counter Mode IP Core

Product Brief

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### Introduction

XIP1111H from Xiphera is a high-throughput Intellectual Property (IP) core implementing the Advanced Encryption Standard (AES) [2] in Galois Counter Mode (GCM) [3]. AES-GCM is a widely used cryptographic algorithm for Authenticated Encryption with Associated Data (AEAD) purposes, as it provides both data confidentiality and authenticity.

XIP1111H has been designed for easy integration with FPGA- and ASIC-based designs in a vendor-agnostic design methodology, and the functionality of XIP1111H does not rely on any FPGA manufacturer-specific features.

### Key Features

- **Moderate** resource requirements: The entire XIP1111H requires approximately 14000 Adaptive Lookup Modules (ALMs) (Intel® Cyclone®V), and does not require any multipliers, DSPBlocks or internal memory in a typical FPGA implementation.
- **Optimized Implementation** utilizing unrolling, pipelining, optimized AES S-box design, and GMAC calculation based on pipelined Karatsuba multipliers enable extremely high performance.
- **Performance:** XIP1111H achieves a throughput in the tens of Gbps range<sup>1</sup>, for example 100+ Gbps in Xilinx® UltraScale+™ MPSoC.
- **Standard Compliance:** XIP1111H is fully compliant with both the Advanced Encryption Algorithm (AES) standard [2], as well as with the Galois Counter Mode (GCM) standard [3].
- **Test Vector Compliance:** XIP1111H passes all test vectors specified in [1].

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<sup>1</sup>As is typical for AEAD algorithms, the highest throughput is achieved for long messages.

- **128-bit Interfaces** ease the integration of XIP1111H with other high-speed FPGA logic.

## Functionality

The main functionality of XIP1111H depends on the mode of operation. When XIP1111H operates in the encryption and authentication tag calculation mode, it encrypts the incoming plaintext blocks into ciphertext blocks, and in addition to this also calculates a 128 bits long authentication tag from both the incoming plaintext and associated data. When XIP1111H operates in the decryption and tag validity checking mode, it decrypts the incoming ciphertext blocks into plaintext blocks, and validates the received authentication tag value by calculating the tag from the incoming ciphertext and associated data blocks and comparing the resulting tag value with the received tag value. As defined by the GCM mode of operation, associated data is included in the authentication tag calculation.

XIP1111H can also operate with zero-length associated data, meaning that XIP1111H treats all signals on the input `data_in` as plaintext to be encrypted or as ciphertext to be decrypted. XIP1111H can also operate with zero-length plaintext or ciphertext, in which case it acts only as an authenticator or authentication validity checker.

XIP1111H outputs first the associated data, followed by encrypted plaintext or decrypted ciphertext (depending on the mode of operation), and as the last output the tag value and associated status signals.

## Block Diagram

The internal high-level block diagram of XIP1111H is depicted in Figure 1.

## Interfaces

The external interfaces of XIP1111H are depicted in Figure 2.

This Product Brief describes a high-level overview of the functionality and capabilities of XIP1111H. Please contact [sales@xiphera.com](mailto:sales@xiphera.com) for a complete datasheet with a detailed description of the input and output signals, startup procedure of XIP1111H, example simulation waveforms, and the FPGA resource requirements of your targeted FPGA family.

## FPGA Resources and Performance

Table 1 presents the FPGA resource requirements for representative implementations on two different FPGA architectures. On request, the resource estimates can also be supplied for other FPGA families.

## Example Use Cases

XIP1111H has several applications, as AES-GCM is a popular AEAD algorithm in a number of standardized communications protocols, including IPSEC, MACSEC and TLS (Transport Layer Security) versions 1.2 and 1.3. Additionally, AES-GCM is used in fibre channel communications and tape storage applications.

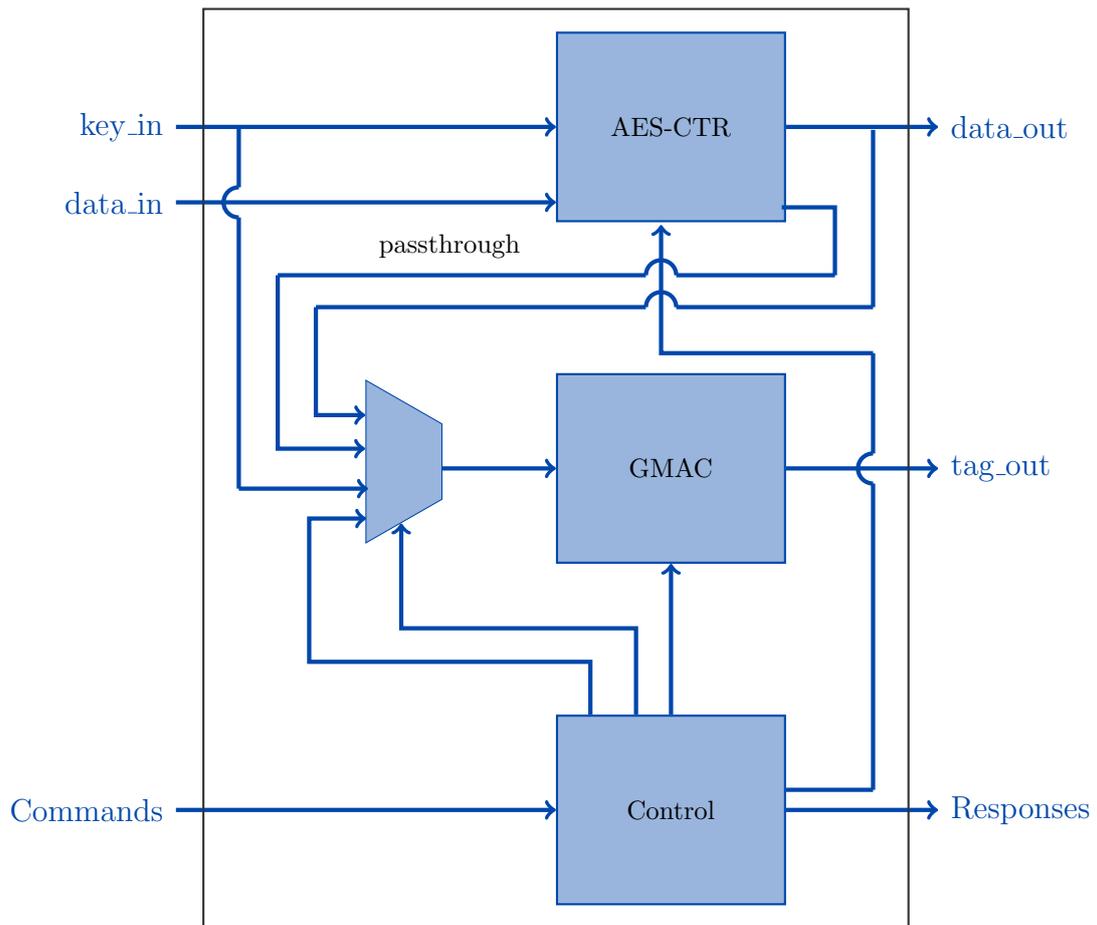


Figure 1: Internal high-level block diagram of XIP1111H

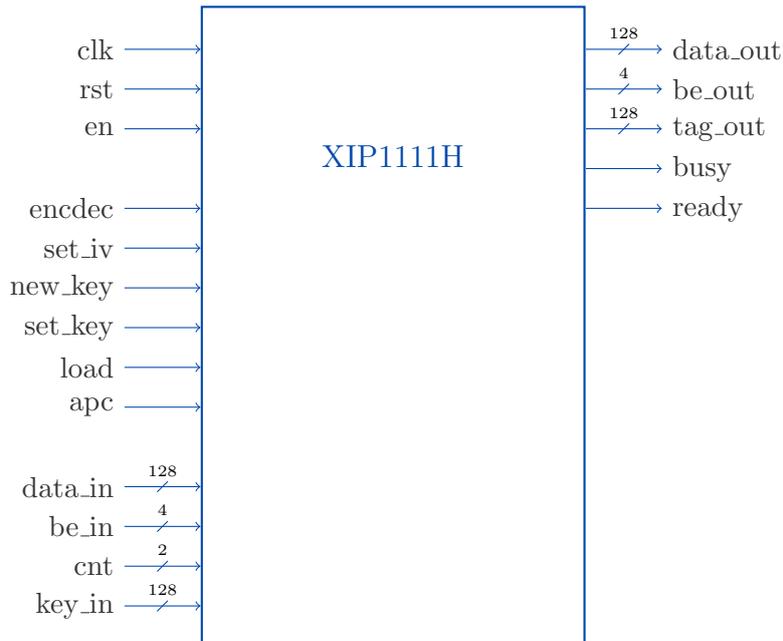


Figure 2: External interfaces of XIP1111H

Device	Resources	$f_{MAX}$	Max. throughput <sup>‡</sup>
Intel <sup>®</sup> Stratix <sup>®</sup> 10 <sup>†</sup>	14604, 10360 REG	404 MHz	51.7 Gbps
Xilinx <sup>®</sup> UltraScale+ <sup>™</sup> MPSoC <sup>*</sup>	16684 LUT	798 MHz	102.1.3 Gbps

<sup>†</sup> Quartus II Prime 19.1., default compilation settings, industrial speedgrade

<sup>\*</sup> Vivado 19.1., default compilation settings, industrial speedgrade

<sup>‡</sup>  $Throughput = f_{MAX} * 128 \text{ bits}$ ; achieved asymptotically with long packets.

Table 1: Resource usage and performance of XIP1111H on representative FPGA families.

## Ordering and Deliverables

Please contact [sales@xiphera.com](mailto:sales@xiphera.com) for pricing and your preferred delivery method. XIP1111H can be shipped in a number of formats, including netlist, source code, or encrypted source code. Additionally, a comprehensive VHDL testbench and a detailed datasheet are included.

## Export Control

XIP1111H protects data confidentiality and is a dual-use product as defined in the Wassenaar Arrangement. Consequently, the export of XIP1111H is controlled by Council Regulation (EC) No 428/2009 of 5 May 2009 and its subsequent changes.

XIP1111H can be immediately shipped to all European Union member states, Australia, Canada, Japan, New Zealand, Norway, Switzerland, United Kingdom, and the United States.

Export to other countries requires authorization from The Ministry for Foreign Affairs of Finland, and a typical processing time for an export authorization is a few weeks.

## About Xiphera

Xiphera specializes in secure and efficient implementations of standardized cryptographic algorithms on Field Programmable Gate Arrays (FPGAs). Our product portfolio includes individual cryptographic Intellectual Property (IP) cores, as well as comprehensive security solutions built from a combination of individual IP cores.

Xiphera is a Finnish company operating under the laws of the Republic of Finland, and is fully owned by Finnish citizens.

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## References

- [1] MACsec GCM-AES Test Vectors. <http://www.ieee802.org/1/files/public/docs2011/bn-randall-test-vectors-0511-v1.pdf>.
- [2] Specification for the Advanced Encryption Standard (AES). Federal Information Processing Standards Publication 197, 2001.
- [3] Morris J. Dworkin. SP 800-38D. Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC. Technical report, Gaithersburg, MD, United States, 2007.